Rev. 10/97

Modified PTO 1082
For Other Than A Small Entity

Attorney Docket No. ALT-155

Applicant(s) : Tony K. Ngai et al.

For : PROGRAMMABLE LOGIC DEVICE HAVING EMBEDDED DUAL-PORT RANDOM ACCESS MEMORY CONFIGURABLE AS SINGLE-PORT MEMORY

EXPRESS MAIL CERTIFICATION

"Express Mail" mailing label number EI187448614US

Date of Deposit July 29, 1998

I hereby certify that this transmittal letter and the other papers and fees identified in this transmittal letter as being transmitted herewith are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and are addressed to the Hon. Assistant Commissioner for Patents, Washington, D.C. 20231.

C CLARKE & SHINTL

Hon. Assistant Commissioner
for Patents
Washington, D.C. 20231

TRANSMITTAL LETTER FOR UNEXECUTED ORIGINAL PATENT APPLICATION

Sir:

Transmitted herewith for filing are the ☒ specification; ☒ claims; ☒ abstract; ☒ unexecuted declaration; for the above-identified patent application.

Also transmitted herewith are:

☒ Four (4) sheets of:

☐ Formal drawings.

☒ Informal drawings. Formal drawings will be filed during the pendency of this application.

The filing fee has been calculated as shown below:

FOR	NUMBER FILED		NUMBER EXTRA		RATE			FEE
BASIC FEE							$	790.00
TOTAL CLAIMS	12	- 20 =	0	x	$ 22	=	$	.00
INDEPENDENT CLAIMS	2	- 3 =	0	x	$ 82	=	$	.00
☐ A MULTIPLE DEPENDENT CLAIM				+	$270	=	$	.00
					TOTAL		$	790.00

☒ A check in the amount of $ 790.00 in payment of the filing fee is transmitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 C.F.R. § 1.16 in connection with the paper(s) transmitted herewith, or credit any overpayment of same, to Deposit Account No. 06-1075. A duplicate copy of this transmittal letter is transmitted herewith.

☐ Please charge $ _____ to Deposit Account No. 06-1075 in payment of the filing fee. A duplicate copy of this transmittal letter is transmitted herewith.

☐ No filing fee is transmitted herewith. The filing fee will be submitted with the executed declaration.

Jeffrey H. Ingerman
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No. EI187448614US

ALT-155

PROGRAMMABLE LOGIC DEVICE HAVING EMBEDDED DUAL-PORT RANDOM ACCESS MEMORY CONFIGURABLE AS SINGLE-PORT MEMORY

Cross Reference to Related Application

This claims the benefit of commonly-assigned United States Provisional Application No. 60/090,358, filed June 23, 1998.

Background of the Invention

This invention relates to a programmable logic device having embedded random access memory. More particularly, this invention relates to such a programmable logic device in which the embedded random access memory is a dual-port memory that can be configured, using resources of the programmable logic device, as a single-port memory.

Programmable logic devices are well known. Such devices typically include a plurality of programmable logic cells or elements arranged on a single integrated circuit chip. A programmable interconnection structure allows a user, typically with the assistance of a dedicated software tool, to configure the device as any type of logic, within the capabilities of the device, that may be required. In order to facilitate the various configurations, the device typically is arranged as a two-dimensional array of logic cells or elements, and typically is provided

with interconnection conductors that run vertically and horizontally within the array, although various ring configurations of conductors are also known. Depending on the design of the particular device, the conductors may run the length or breadth of the device, or may span only a portion of the device; many devices have combinations of conductors of various types. Whatever their type, conductors usually run in parallel groups or groups. The interconnection conductors are complemented by programmable interconnection resources that allow various conductors to be connected together and to particular inputs or outputs of the various logic cells or elements.

In early programmable logic devices, the programmable interconnection resources included fully populated matrices where interconnection conductors crossed, allowing any conductor in one group of interconnection conductors to be connected to any conductor in the intersecting group of interconnection conductors. As programmable logic devices became larger in size, it became impractical to provide such fully populated interconnections, because of the physical space they required on the integrated circuit chip. In current devices, it is common for most programmable interconnection resources to be less than fully populated. For example, in many cases, programmable interconnection resources are provided in the form of multiplexers. Using statistical techniques, based on likely user requirements, sufficient programmable interconnection resources are provided so that substantially any signal routing that a user might want to implement will be possible using some combination of interconnection conductors and programmable interconnection resources.

It has become common to provide on-board random access memory (RAM) as part of programmable

logic devices. This particularly true in, but is not limited to, programmable logic devices whose logic elements are based on look-up tables implemented in static random access memory (SRAM). When RAM is provided on a programmable logic device, it may be configurable as logic elements, or it may be used to satisfy other memory requirements of the end user's logic configuration.

It is known to provide single-port RAM -- i.e., RAM having a single port through which both read and write operations are conducted -- on a programmable logic device. It is also known to combine two blocks of single-port RAM on a programmable logic device to emulate dual-port RAM -- i.e., RAM having separate ports for reading and writing thereby allowing simultaneous read and write operations. One way of emulating dual-port RAM is to write all data to be stored in the RAM into both single-port RAM blocks, but to read from only one of the RAM blocks. This requires directing both addressing signals and data to be stored to both RAM blocks. An alternative approach is to use a single single-port RAM block to emulate a dual-port RAM by time-multiplexing read and write operations. However, this approach reduces by half the effective speed of the RAM. Using either approach, the various signals and data must be routed to the proper ports via the programmable interconnect structure of the programmable logic device.

It would be desirable to be able to provide a programmable logic device having embedded random access memory that can function equally well in either single-port or dual-port operation.

Summary of the Invention

It is an object of the invention to provide a programmable logic device having embedded random access memory that can function equally well in either single-port or dual-port operation.

In accordance with the present invention, there is provided a programmable logic device having a plurality of logic resources, a plurality of groups of interconnection conductors for interconnecting the logic resources, and a plurality of programmable interconnection resources for connecting conductors in the groups of interconnection conductors to one another and to the plurality of logic resources, with the programmable interconnection resources being less than fully populated. The programmable logic device further includes at least one random access memory having a read port and a write port, a first programmable interconnection resource in the plurality of programmable interconnection resources for connecting port conductors in the read port to a selected one of the plurality of groups of interconnection conductors, and a second programmable interconnection resource in the plurality of programmable interconnection resources for connecting port conductors in the write port to the selected one of the plurality of groups of interconnection conductors. The first and second programmable interconnection resources are populated to allow connection of an individual conductor in the selected one of the plurality of groups of interconnection conductors to corresponding port conductors in both the read port and the write port.

The present invention achieves faster speeds for dual-port RAM in a programmable logic device by providing a true dual-port RAM. This eliminates the need to time-multiplex read and write operations, and

therefore effectively doubles the speed available in previous programmable logic devices in which a single-port RAM was used with time-multiplexing of read and write operations on the same port. Alternatively, this eliminates the waste of using two RAMS to emulate a single RAM as described above.

When the dual-port RAM provided in accordance with the present invention is used in a programmable logic device of the type described above, each port must be connected to the interconnect structure of the programmable logic device so that signals can be sent to and received from the RAM. This presents potential difficulties, because, although in the present invention dual-port RAM is provided in a programmable logic device in the place of single-port RAM as previously known in programmable logic devices, there may be instances when the user's desired configuration requires the availability of single-port RAM. As described above, in many types of programmable logic devices the programmable interconnection resources are not fully populated. Thus, the port conductors in the read and write ports of a dual-port RAM provided in accordance with the present invention might not be connectable to the same group of conductors, and even if they are they might not be connectable to the same conductors within that group of conductors.

Therefore, in accordance with the present invention, both ports of the dual-port RAM are connected to programmable interconnection resources that connect them to the same group of conductors. Moreover, the programmable interconnection resources are populated in such a way that each pair of corresponding port conductors in the two ports can be connected the same individual conductor in the associated group of conductors.

Accordingly, if a user configuration of the programmable logic device requires the availability of single-port RAM, the programmable interconnection resources are configured so that corresponding read port conductors and write port conductors are connected to the same interconnection conductors of the programmable logic device. Then, in operation, the remainder of the circuit sends either a read address signal or a write address signal, as the case may be, to what it sees as a single destination just as it would with a standard single-port RAM. In fact, identical signals arrive at the two separate ports, but only the signals at one port are acted upon, in accordance with a read/write selection or enable signal that the circuit sends to enable either the read operation or the write operation of what it "thinks" is a single port. Thus, to the remainder of the programmable logic device, the dual-port RAM "looks" like a single-port RAM, using all of the same signals as a conventional single-port RAM.

According to a first preferred embodiment, the programmable interconnection resources for the read port and the write port are, at least with respect to the read and write ports, identically populated -- i.e., the programmable interconnection resources are provided such that each port conductor in one of the ports can be connected to all of the same interconnection conductors to which the corresponding conductor in the other of the ports can be connected. It is not necessary according to this embodiment of the invention, however, for the programmable interconnection resources to be identically populated with respect to other interconnection conductors not used by either port, although such completely identical population of the programmable interconnection resources is within the present invention.

In a second preferred embodiment according to the invention, the programmable interconnection resources for the read port and the write port are not identically populated even with respect to the ports themselves. In this embodiment, each port conductor in one of the ports can be connected to at least one interconnection conductor to which the corresponding port conductor in the other of the ports can be connected, but corresponding port conductors might not share all of the same interconnection conductors.

Both of the aforementioned embodiments allow the dual-port RAM provided in accordance with the present invention to function as a single-port RAM by providing at least one combination of conductor assignments that allows identical address and control signals to reach both ports. The first embodiment allows more than one such possible set of conductor assignments, increasing flexibility in configuring the dual-port RAM of the device as single-port RAM, at possible expense of flexibility in configuring other functions of the overall programmable logic device. The second embodiment provides the reverse, allowing a smaller number, or perhaps only one, possible configuration of the dual-port RAM as a single-port RAM, but increasing flexibility in programming other functions of the overall programmable logic device.

Brief Description of the Drawings

The above and other objects and advantages of the invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout, and in which:

FIG. 1 is a high-level diagram of a programmable logic device including embedded dual-port

random access memory configured according to the present invention;

FIG. 2 is a block diagram of an example of a dual-port random access memory configured according to the present invention;

FIGS. 3A and 3B are schematic representations of possible arrangements of the programmable interconnection resources of FIG. 2; and

FIG. 4 is a simplified block diagram of an illustrative system employing a programmable logic device incorporating dual-port random access memory configured in accordance with the invention.

Detailed Description of the Invention

FIG. 1 shows, as an example of a device in which the present invention can be used, a programmable logic device 10 having embedded random access memory. It should be recognized, however, that the present invention can be used with other types of programmable logic devices having random access memory embedded therein. For example, the invention could be used with programmable logic devices (not shown) similar to those described generally in Freeman U.S. Patent Re. 34,363, which is also hereby incorporated by reference herein in its entirety.

As can be seen, device 10 has a plurality of random access memory arrays 11, which are arranged in one column on device 10. The remaining columns of device 10 are populated by programmable logic regions 12. Each row has two groups of horizontal interconnection conductors 13 that extend the entire length of the row, one group of conductors 13 being above the row and the other group being below the row. Conductors 13 are sometimes referred to as full-horizontal conductors or as global horizontal conductors. Each row also has four groups of

horizontal interconnection conductors 14 that extend along half the length of the row. Two of these groups extend respectively along the top and bottom of the left half of the row. The other two groups of these conductors 14 extend respectively along the top and bottom of the right half of the row. The conductors 14 associated with each half of a row are preferably not directly connectable to the conductors 14 associated with the other half of the row. Conductors 14 are sometimes referred to as half-horizontal conductors. Each column of regular logic regions 12 has a group of vertical interconnection conductors 15 that extend continuously or substantially continuously along the entire length of the column.

In order to feed logic signals to each region 12, each regular logic region has an associated plurality of region feeding conductors 16 that can bring signals to the logic region from the horizontal conductors 13 and 14 associated with that region. Each region 12 also has eight associated local feedback conductors 17. Each conductor 17 makes the output signal of a respective one of the logic modules 18 in the associated region 12 available as an input to any of the other logic modules in that region without having to use any programmable interconnection resources that are not exclusively associated with the region.

Each region 12 also has output conductors 19 for conveying the output logic signals of the logic modules 18 in that region to the associated conductors 13 and 14. Programmable logic connectors ("PLCs") (not shown) are associated with each regular logic region 12 for making connections from the vertical (15) to the horizontal (13 and 14) conductors associated with the region. A plurality of output

networks 100 connect the various conductors (13-15) to input/output pins 101.

Any one or more of random access memory arrays 11 can be a dual-port RAM configured according to the present invention. It is not required in accordance with the present invention that all random access memory arrays 11 provided in a programmable logic device be dual-port RAMs. However, the invention is most useful when there are no single-port RAMs provided in the device; when single-port RAMs are provided, there is little need to configure a dual-port RAM as a single-port RAM. By the same token, not all dual-port RAMs in a device need be configured in accordance with the invention, as long as enough so configured are available to satisfy the expected need by users to emulate single-port RAM.

FIG. 2 shows in detail a preferred configuration of a dual-port RAM 11 according to the present invention. As shown, dual-port RAM 11 is a 64x32 random access memory array (although the present invention could be used to equal advantage with RAM arrays of substantially any size) having write port 20 to the left and read port 21 to the right, located below groups 13, 14 of horizontal interconnection conductors. In one preferred embodiment, groups 13, 14 might encompass, between them, about 200 conductors, which could be thought of collectively as a conductor bus.

In the embodiment shown in FIG. 2, twenty-two write port conductors 23 are connected to horizontal conductors 13, 14 by programmable interconnection resource 22, while twenty-two read port conductors 25 are connected to horizontal conductors 13, 14 by programmable interconnection resource 24. Programmable interconnection resources 22, 24 are preferably less than fully populated interconnection matrices or

multiplexers, or similar structures, as are well known in programmable logic devices.

Write port conductors 23 pass through a first programmable interconnect array ("PIA") 26 to a first control/flip-flop block 27 which includes control logic (not shown) of a type that is well known for directing write address signals and write data to the appropriate inputs of RAM 11, as well as one or more flip-flops to register the write address signals and/or data for synchronous writing as controlled by clock and/or enable signals. The clock and enable signals may be provided on conductors 23 or on other conductors (not shown) that provide those signals device-wide.

Control/flip-flop block 27 directs write address row signals 29 to write address row decoder 28. For the 64-row array 11 shown in FIG. 2, write address row signals 29 include six bits ($2^6 = 64$). Similarly, control/flip-flop block 27 directs write address column signals 200 to write address column decoder 201. For the 32-column array 11 shown in FIG. 2, write address column signals 200 include five bits ($2^5 = 32$). Control/flip-flop block 27 also directs write data signals 202 to read/write data buffer 203.

Read port conductors 25 pass through a second programmable interconnect array ("PIA") 26' to a second control/flip-flop block 27' which includes control logic (not shown), similar to that of block 27, of a type that is well known for directing read address signals to the appropriate inputs of RAM 11, and registering those signals for synchronous operation as required.

Control/flip-flop block 27' directs read address row signals 29' to read address row decoder 28'. For the 64-row array 11 shown in FIG. 2, read address row signals 29' include six bits ($2^6 = 64$). Similarly, control/flip-flop block 27' directs

read address column signals 200' to read address column decoder 201'. For the 32-column array 11 shown in FIG. 2, read address column signals 200' include five bits ($2^5 = 32$). Signals 200' preferably also include a read-enable signal which controls whether read port 21 is activated. If the read-enable signal is high, read data signals 202' preferably are selected by multiplexer 204 and buffered by tristate device 205 and routed to the desired destination through the programmable interconnect structure of device 10.

When RAM array 11 is to be used as a single-port RAM, the user's configuration will send read address signals and write address signals to what appears, according to that configuration, to be a single destination. In fact, of course, write address signals must arrive at write port 20, while read address signals must arrive at read port 21. Therefore, because both read address signals and write address signals are sent along the same ones of conductors 13, 14 (because the user configuration "thinks" the signals go to the same place), corresponding read port conductors and write port conductors must be able to be connected to the same ones of conductors 13, 14. For example, if the seventeenth one of write port conductors 23 can be connected to the 103rd, the 156th and the 192nd ones of conductors 13, 14, then the seventeenth one of read port conductors 25 must be able to be connected to at least one of the 103rd, the 156th and the 192nd ones of conductors 13, 14 in order for device 10 to be able to be configured for RAM array 11 to be used as a single-port RAM. This is accomplished in accordance with the invention by arranging the available pattern of connections when constructing the less than fully populated programmable interconnection resources 22, 24 to assure that the necessary connections are available.

As set forth above, programmable interconnection resources 22, 24 can be constructed so that the available interconnections for write conductors 23 and read conductors 25 vis-à-vis conductors 13, 14 are identical, to provide multiple combinations for single-port emulation, or so that the available interconnections merely overlap to provide at least one combination for single-port emulation. These two alternatives are illustrated schematically in FIGS. 3A and 3B.

FIG. 3A shows schematically the first alternative, in which programmable interconnection resources 22, 24 are identically populated, at least as far as the intersections of interconnection conductors 13, 14 with port conductors 23, 25 are concerned (i.e., there may be other interconnections within those programmable interconnection resources that are not shown). In FIG. 3A, interconnection conductors 13, 14 are represented by the six individual conductors 13a, 13b, 13c, 13d, 13e and 13f, while port conductors 23, 25 are represented by individual conductors 23a, 23b and 23c, and 25a, 25b and 25c, respectively.

In this embodiment, in an arrangement shown for illustrative purposes only, within programmable interconnection resource 22, conductor 23a can be connected to any of conductors 13b, 13c or 13e, conductor 23b can be connected to any of conductors 13c, 13d or 13f, and conductor 23c can be connected to any one of conductors 13b, 13d or 13e. Programmable interconnection resource 24 is identically populated with respect to the intersection of interconnection conductors 13, 14 with port conductors 25. Thus, within programmable interconnection resource 24, conductor 25a, corresponding to conductor 23a, can be connected to any

of conductors 13b, 13c or 13e; conductor 25b, corresponding to conductor 23b, can be connected to any of conductors 13c, 13d or 13f; and conductor 25c, corresponding to conductor 23c, can be connected to any one of conductors 13b, 13d or 13e.

FIG. 3B shows schematically the second alternative, in which programmable interconnection resources 22, 24 are not identically populated, but, at least as far as the intersections of interconnection conductors 13, 14 with port conductors 23, 25 are concerned (i.e., there may be other interconnections within those programmable interconnection resources that are not shown), merely have overlapping populations of available interconnections. In FIG. 3B, as in FIG. 3A, interconnection conductors 13, 14 are represented by the six individual conductors 13a, 13b, 13c, 13d, 13e and 13f, while port conductors 23, 25 are represented by individual conductors 23a, 23b and 23c, and 25a, 25b and 25c, respectively.

In this embodiment, in an arrangement shown for illustrative purposes only, within programmable interconnection resource 22, conductor 23a can be connected to any of conductors 13b, 13c or 13e, conductor 23b can be connected to any of conductors 13c, 13d or 13f, and conductor 23c can be connected to any one of conductors 13b, 13d or 13e. Within programmable interconnection resource 24, conductor 25a, corresponding to conductor 23a, can be connected to any of conductors 13d, 13e or 13f; conductor 25b, corresponding to conductor 23b, can be connected to any of conductors 13b, 13c or 13d; and conductor 25c, corresponding to conductor 23c, can be connected to any one of conductors 13a, 13b or 13c. Thus, corresponding port conductors 23a and 25a have only one available connection in common to interconnection conductor 13e, corresponding port

conductors 23b and 25b have two available connections in common to interconnection conductors 13c and 13d, and corresponding port conductors 23c and 25c have only one available connection in common to interconnection conductor 13b.

It should be noted that the "interiors" of programmable interconnection resources 22, 24 as shown in FIGS. 3A, 3B are schematic only, and programmable interconnection resources 22, 24 may be constructed using any new or previously known structure for achieving such connections.

FIG. 4 illustrates a programmable logic device 10 incorporating RAM arrays 11 configured according to this invention in a data processing system 400. Data processing system 400 may include one or more of the following components: a processor 401; memory 402; I/O circuitry 403; and peripheral devices 404. These components are coupled together by a system bus 405 and are populated on a circuit board 406 which is contained in an end-user system 407.

System 400 can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. Programmable logic device 10 can be used to perform a variety of different logic functions. For example, programmable logic device 10 can be configured as a processor or controller that works in cooperation with processor 401. Programmable logic device 10 may also be used as an arbiter for arbitrating access to a shared resource in system 400. In yet another example, programmable logic device 10 can be configured as an interface between processor 401 and one of the other components in system 400. It should be noted that system 400 is only exemplary, and that the true scope

and spirit of the invention should be indicated by the following claims.

Various technologies can be used to implement programmable logic devices 10 employing the RAM arrays 11 configured according to this invention, as well as the various components of those RAM arrays. Moreover, this invention is applicable to both one-time-only programmable and reprogrammable devices.

Thus it is seen that a programmable logic device having embedded random access memory that can function equally well in either single-port or dual-port operation is provided. One skilled in the art will appreciate that the present invention can be practiced by other than the described embodiments, which are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.

WHAT IS CLAIMED IS:

1. A programmable logic device comprising:

a plurality of logic resources;

a plurality of groups of interconnection conductors for interconnecting said logic resources; and

a plurality of programmable interconnection resources for connecting conductors in said groups of interconnection conductors to one another and to said plurality of logic resources, said programmable interconnection resources being less than fully populated; said programmable logic device further comprising:

at least one random access memory having a read port and a write port;

a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port to a selected one of said plurality of groups of interconnection conductors; and

a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port to said selected one of said plurality of groups of interconnection conductors; wherein:

said first and second programmable interconnection resources are populated to allow connection of an individual conductor in said selected one of said plurality of groups of interconnection conductors to corresponding port conductors in both said read port and said write port.

2. The programmable logic device of claim 1 wherein said first and second programmable interconnection resources are identically populated.

3. A digital processing system comprising:

processing circuitry;

a system memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 1 coupled to the processing circuitry and the system memory.

4. A printed circuit board on which is mounted a programmable logic device as defined in claim 1.

5. The printed circuit board defined in claim 4 further comprising:

a board memory mounted on the printed circuit board and coupled to the programmable logic device.

6. The printed circuit board defined in claim 5 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the board memory.

7. An integrated circuit comprising:

a plurality of semiconductor devices;

a plurality of groups of interconnection conductors for interconnecting said semiconductor devices; and

a plurality of programmable interconnection resources for connecting conductors in said groups of interconnection conductors to one another and to said plurality of semiconductor devices, said programmable interconnection resources being less than fully populated; said integrated circuit further comprising:

at least one random access memory having a read port and a write port;

a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port to conductors in a selected one of said plurality of groups of interconnection conductors; and

a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port to conductors in said selected one of said plurality of groups of interconnection conductors; wherein:

said first and second programmable interconnection resources are populated to allow connection of an individual conductor in said selected one of said plurality of groups of interconnection conductors to corresponding port conductors in both said read port and said write port.

8. The integrated circuit of claim 7 wherein said first and second programmable interconnection resources are identically populated.

9. A digital processing system comprising:

processing circuitry;

a system memory coupled to said processing circuitry; and

an integrated circuit as defined in claim 7 coupled to the processing circuitry and the system memory.

10. A printed circuit board on which is mounted a programmable logic device as defined in claim 7.

11. The printed circuit board defined in claim 10 further comprising:

a board memory mounted on the printed circuit board and coupled to the integrated circuit.

12. The printed circuit board defined in claim 11 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the board memory.

PROGRAMMABLE LOGIC DEVICE HAVING EMBEDDED DUAL-PORT RANDOM ACCESS MEMORY CONFIGURABLE AS SINGLE-PORT MEMORY

Abstract of the Disclosure

A programmable logic device has embedded random access memory ("RAM") that can function equally well in either single-port or dual-port operation. The RAM is dual-port RAM whose read address inputs and write address inputs are both connected to a conductor bus via two different sparsely populated programmable interconnection resources. The programmable interconnection resources are arranged so that each pair of corresponding read address and write address inputs can be connected to at least one conductor in common on the conductor bus, allowing the RAM to be configured to mimic a single-port RAM as read address signals and write address signals originating at remote components of the programmable logic device "think" they are being directed to the same address inputs.

DECLARATION AND POWER OF ATTORNEY

We, Tony K. Ngai, Rakesh H. Patel, Srinivas T. Reddy, and Richard G. Cliff, declare that we are citizens, respectively, of Canada, the United States of America, India, and the United States of America, respectively residing and having post office addresses at 2830 Gazelle Drive, Campbell, California 95008, 20087 Las Ondas Court, Cupertino, California 95104, 2289 Camellia Court, Fremont, California 94539, and 194 Smithwood Street, Milpitas, California 95035;

that we verily believe ourselves to be the original, first and joint inventors of the invention or discovery in:

PROGRAMMABLE LOGIC DEVICE HAVING
EMBEDDED DUAL-PORT RANDOM ACCESS MEMORY
CONFIGURABLE AS SINGLE-PORT MEMORY

which is described and claimed in the attached specification, and for which a patent is sought;

that we have reviewed and do understand the content of said specification, including the claims, and acknowledge our duty to disclose to the United States Patent and Trademark Office information known by us to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

that we do not know and do not believe that this invention or discovery was ever known or used in the United States of America before our invention or discovery thereof, or patented or described in any printed publication in any country before our invention or discovery thereof, or more than one year prior to this application; or in public use or on sale in the

United States of America more than one year prior to this application; that this invention or discovery has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by us or our legal representatives or assigns more than twelve months prior to this application; and that no application for patent or inventor's certificate on this invention or discovery has been filed in any country foreign to the United States of America by us or our legal representatives or assigns;

We hereby claim the benefit under Title 35, United States Code, § 119(e), of United States Provisional Application No. 60/090,358, filed June 23, 1998;

and we hereby appoint Robert R. Jackson, Esq., Reg. No. 26,183, and Jeffrey H. Ingerman, Esq., Reg. No. 31,069, our attorneys, with power of substitution, and with power of appointment of associate attorneys and agents, and of revocation of their powers, to prosecute this application and any divisions, continuations in whole or in part, renewals and reissues of the same, and to transact all business in the Patent and Trademark Office connected therewith;

and we request that communications be sent to:

Jeffrey H. Ingerman
Fish & Neave
1251 Avenue of the Americas
New York, New York 10020-1104

and that telephone calls be directed to:

Jeffrey H. Ingerman
(212) 596-9000.

Wherefore, we pray that Letters Patent be granted to us for the invention or discovery described and claimed in the attached specification and claims, and we hereby subscribe our names to the foregoing specification and claims, declaration, and power of attorney.

We declare, further, that we understand the English language and that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date	Tony K. Ngai
Date	Rakesh H. Patel
Date	Srinivas T. Reddy
Date	Richard G. Cliff

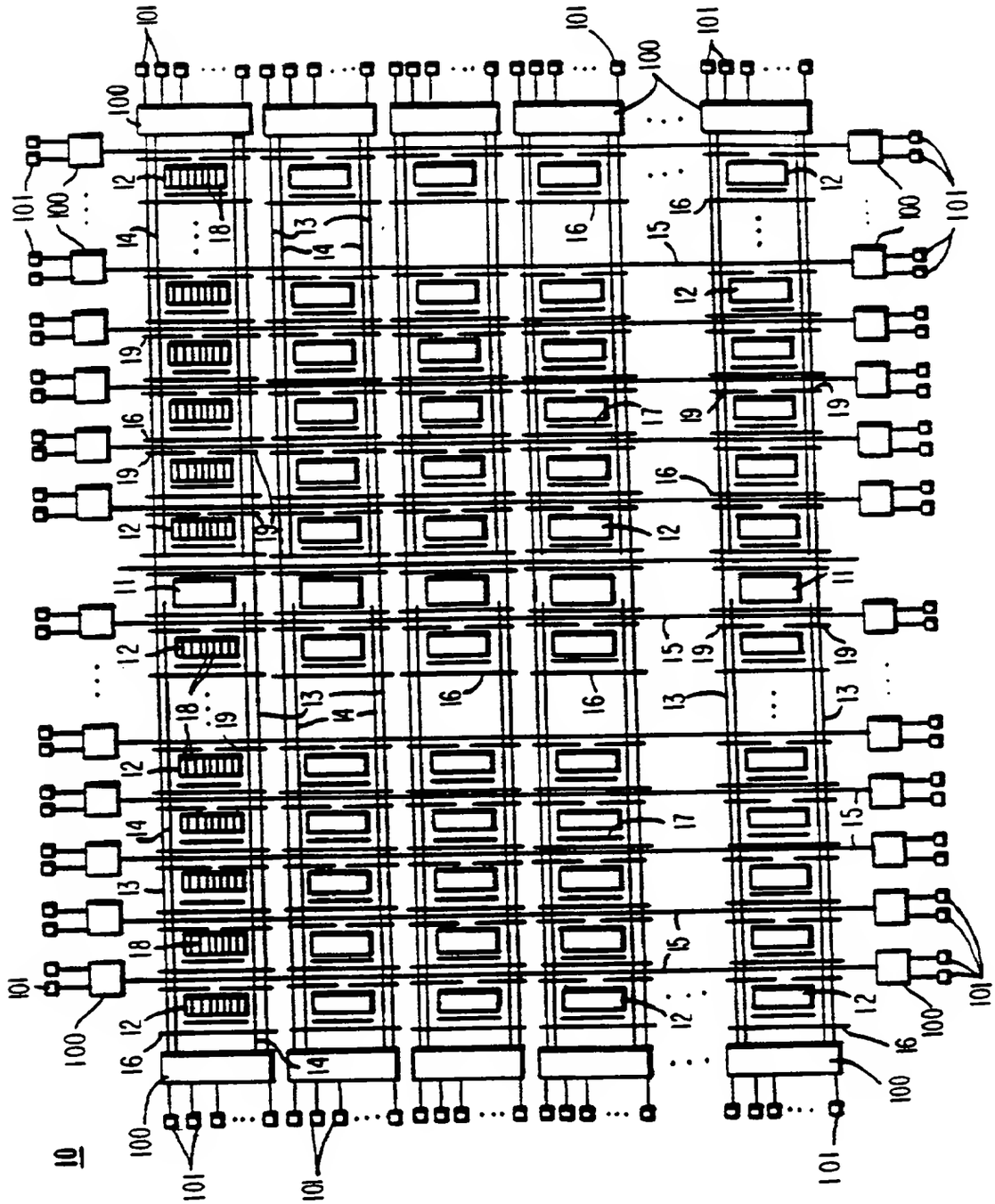
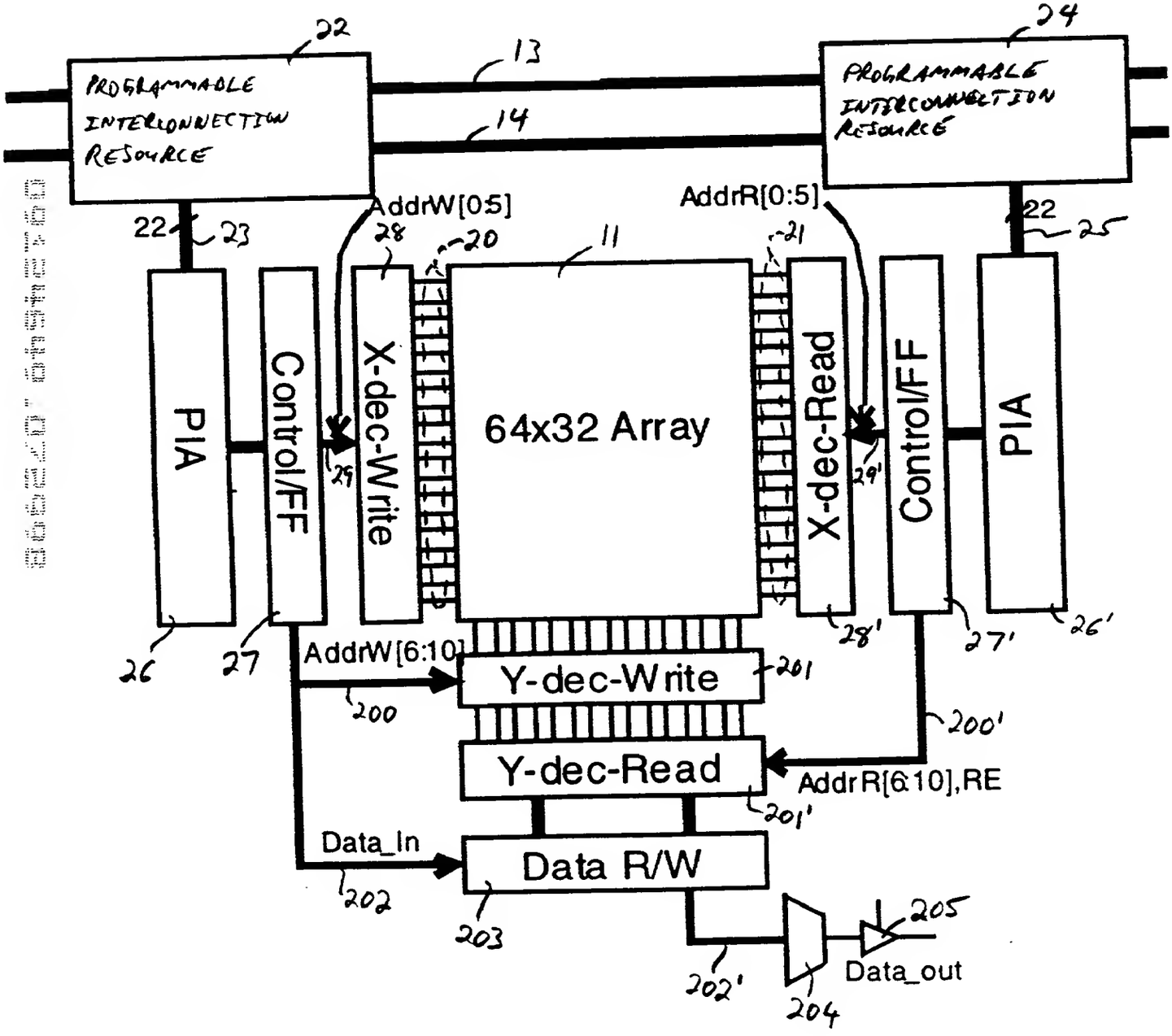


FIG. 1

FIG. 2


PROGRAMMABLE INTERCONNECTION RESOURCE
PROGRAMMABLE INTERCONNECTION RESOURCE
22
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14
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AddrW[0:5]
AddrR[0:5]
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22
25
PIA
Control/FF
X-dec-Write
64x32 Array
X-dec-Read
Control/FF
PIA
29
29'
26
27
28'
27'
26'
AddrW[6:10]
Y-dec-Write
201
200
200'
Y-dec-Read
AddrR[6:10],RE
201'
Data_In
Data R/W
202
203
205
202'
Data_out
204

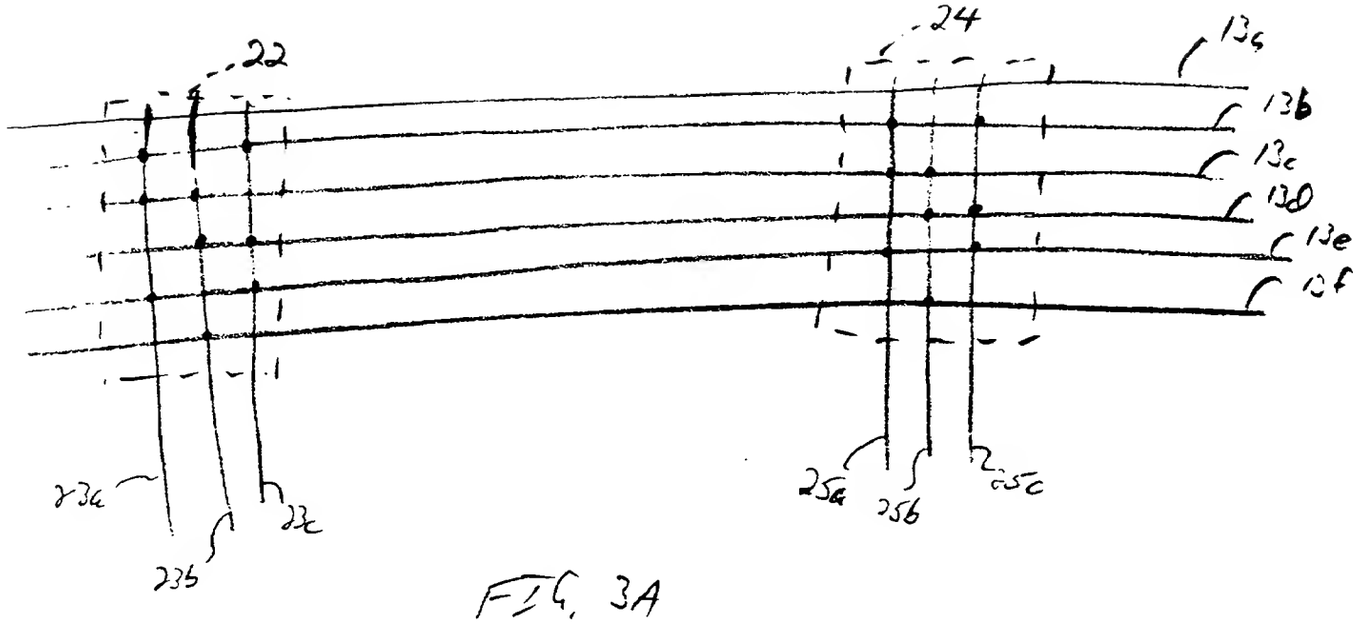

22
24
13a
13b
13c
13d
13e
13f
23a
23b
23c
25a
25b
25c

FIG. 3A

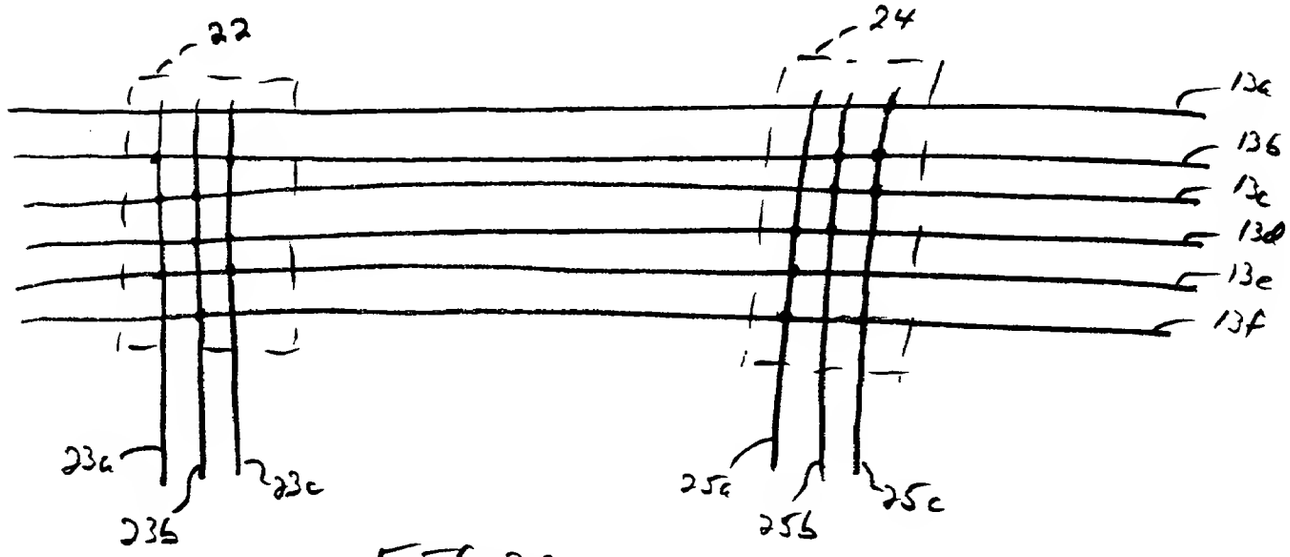
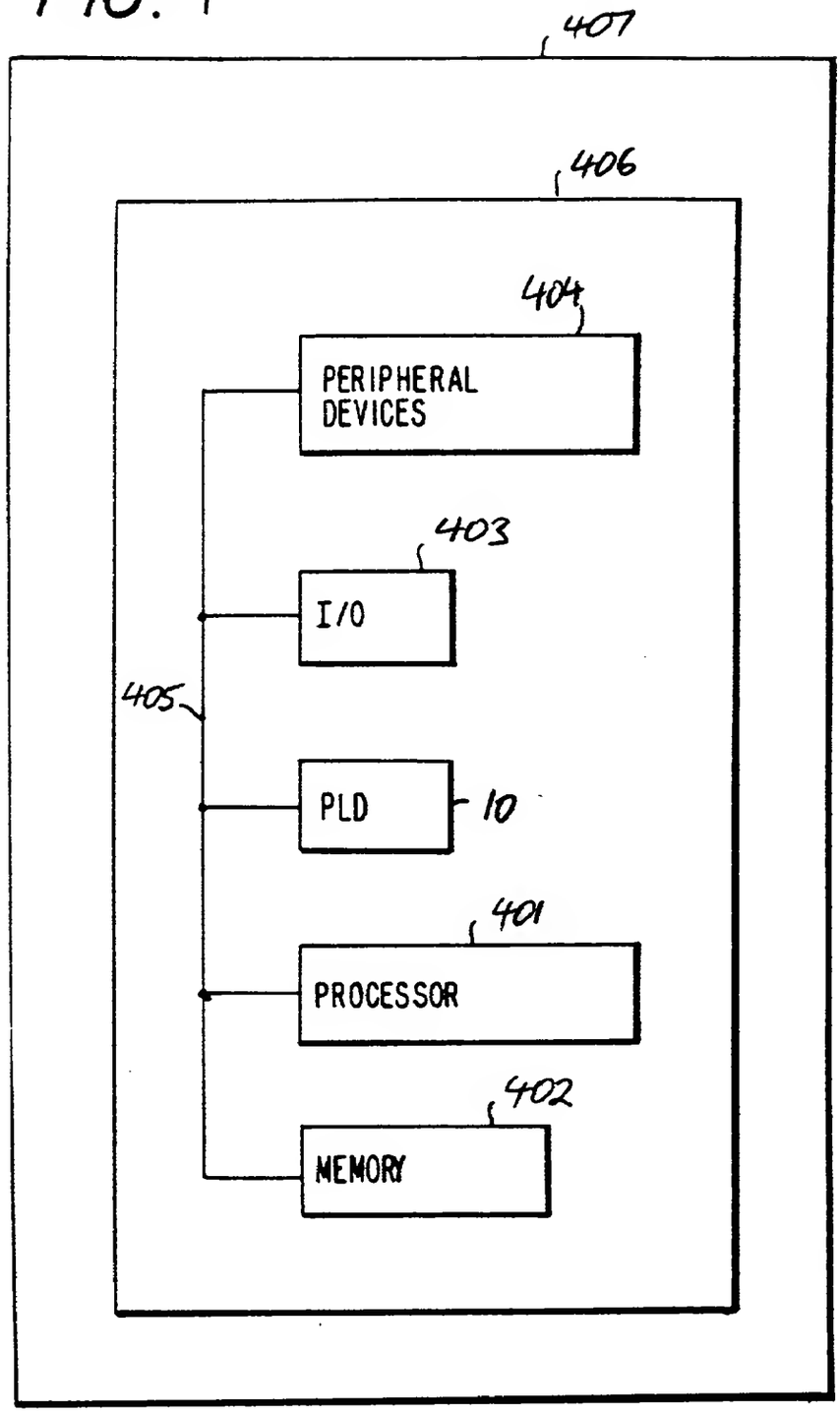

22
24
13a
13b
13c
13d
13e
13f
23a
23b
23c
25a
25b
25c

FIG. 3B

FIG. 4


407
406
404
PERIPHERAL DEVICES
403
I/O
405
PLD
10
401
PROCESSOR
402
MEMORY

400